Intel Mask Competitive Advantages

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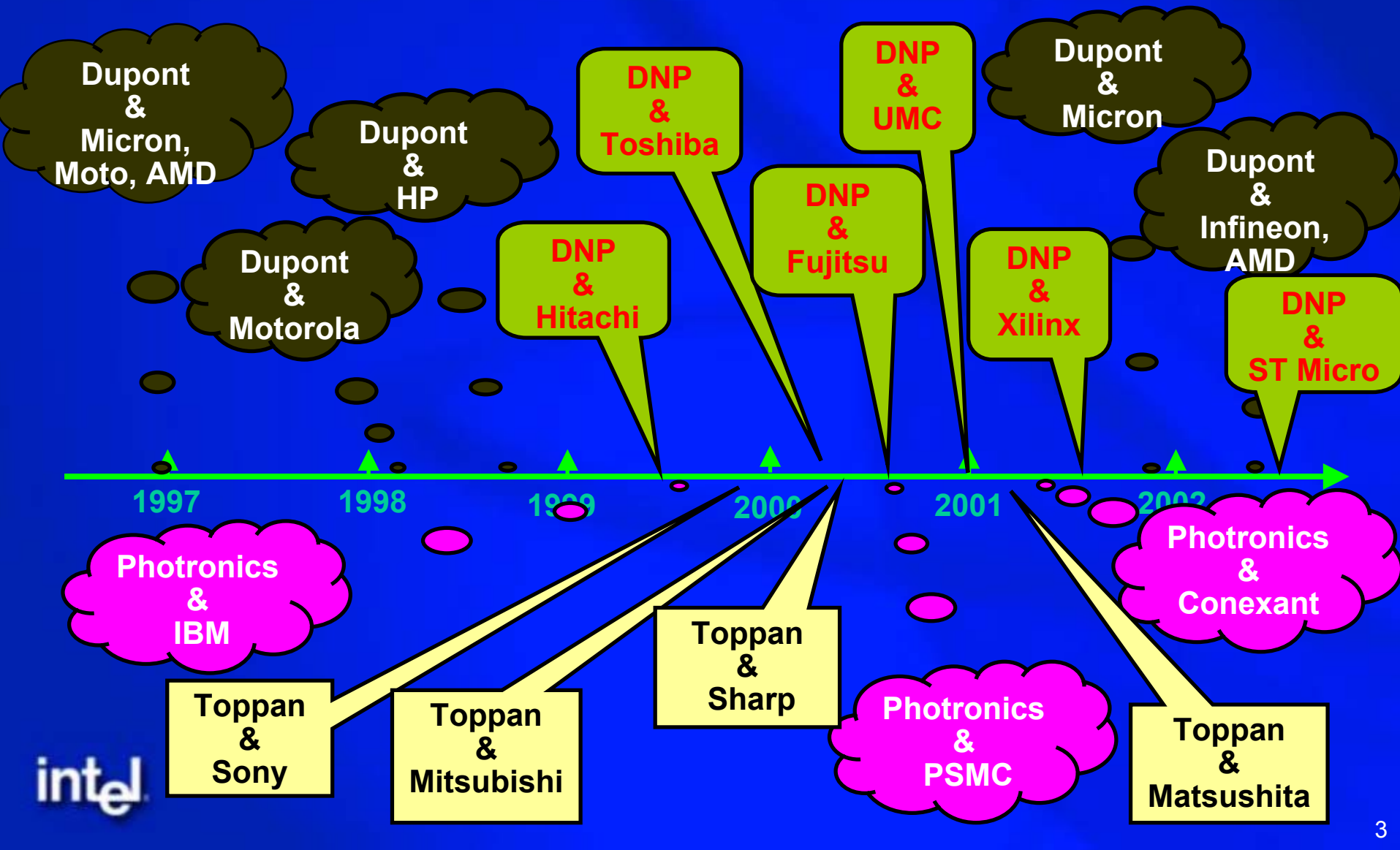
What do we want to communicate?

- Intel ***internal mask shop*** provides major competitive advantages.
- Intel has developed world leading ***65nm node masks*** enabling Intel Silicon process development and continue the 2-year technology cycle.

Mask Industry Landscape Changes

- Alliance formation with ***captive mask shops exiting***



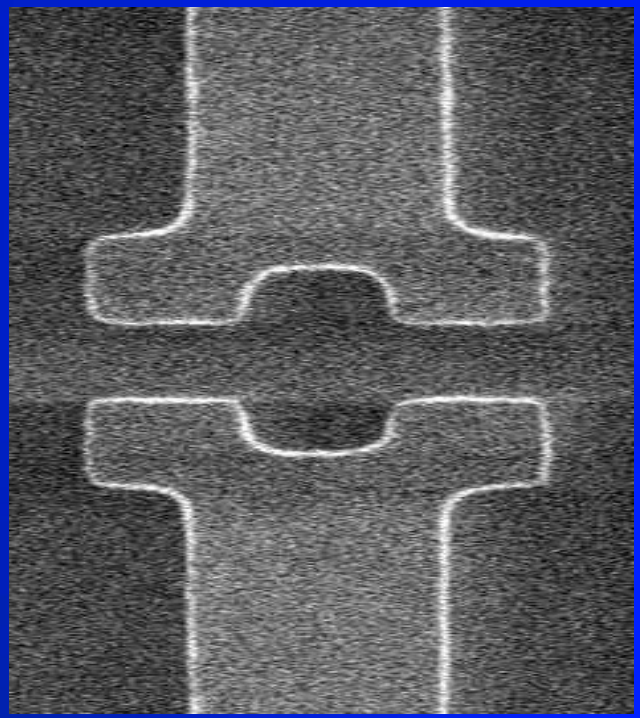
Intel Continues to *INVEST* in Internal Mask Shop

Intel has the financial strength and economy of scale to fund & drive maximum differentiation

- **Intel Mask Competitive Advantages:**
  - Leading edge capabilities
  - Fast TPT (Throughput Time)
  - Integrated services & solutions
  - Mask cost advantage

World Leading Transistor Gate Patterning Capability

- Industry leading 50nm transistor: small gate patterning
- World best mask gate CD (critical dimension) uniformity



Gate Mask for
50nm Transistor

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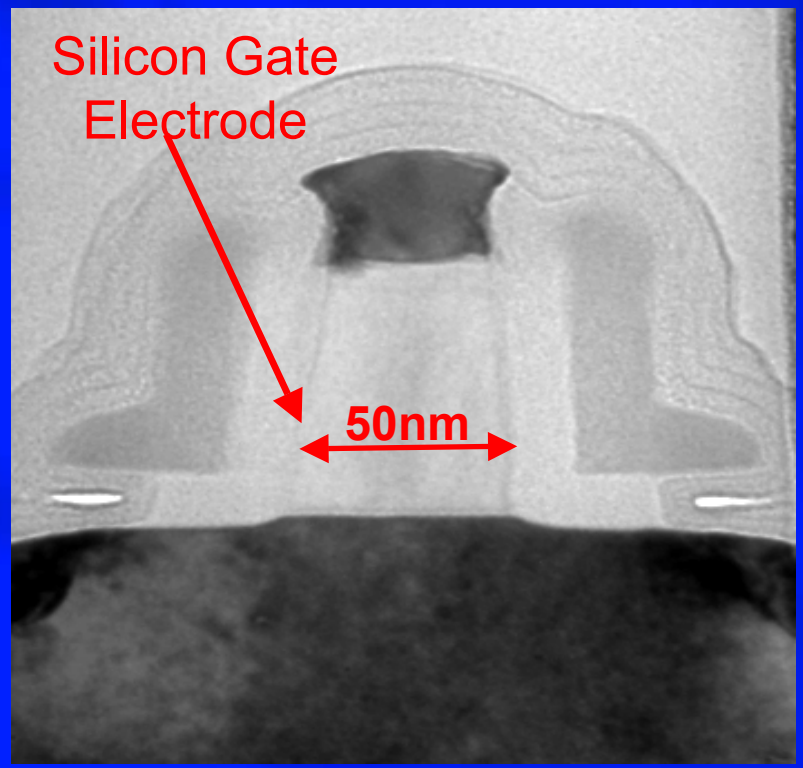
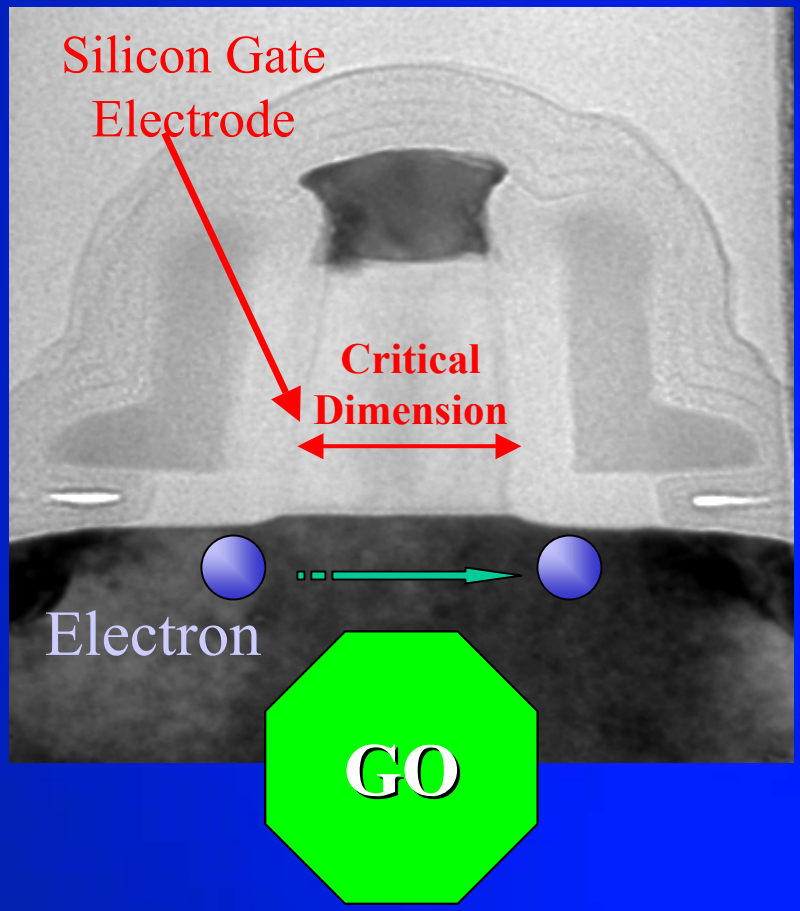
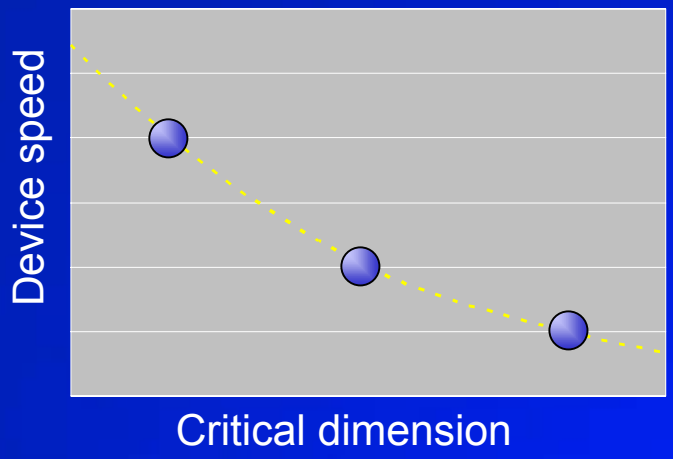


50 nm transistor dimension is ~2000x smaller than diameter of human hair

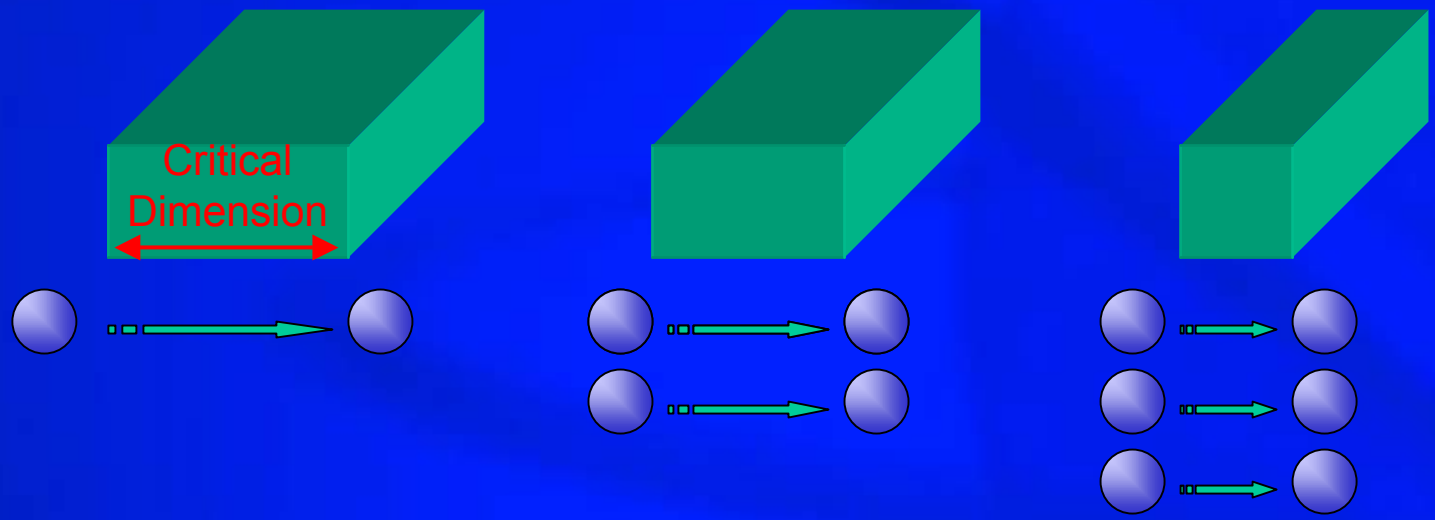


When the transistor is switched on, electrons move across the silicon gate electrode.

The critical dimension is the width of the gate and the distance that the electrons must traverse.



More electrons are able to move across shorter distances in shorter amounts of time.

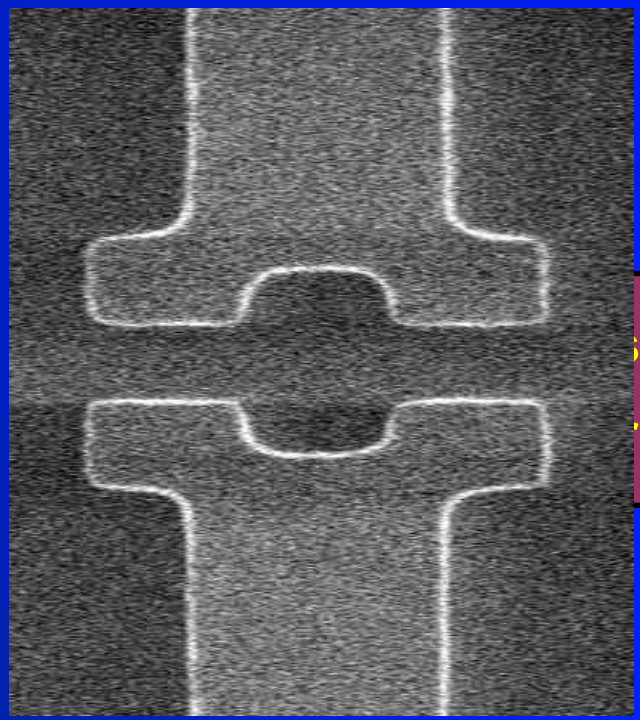


Shorter gates (*smaller feature sizes*) yield faster transistors.

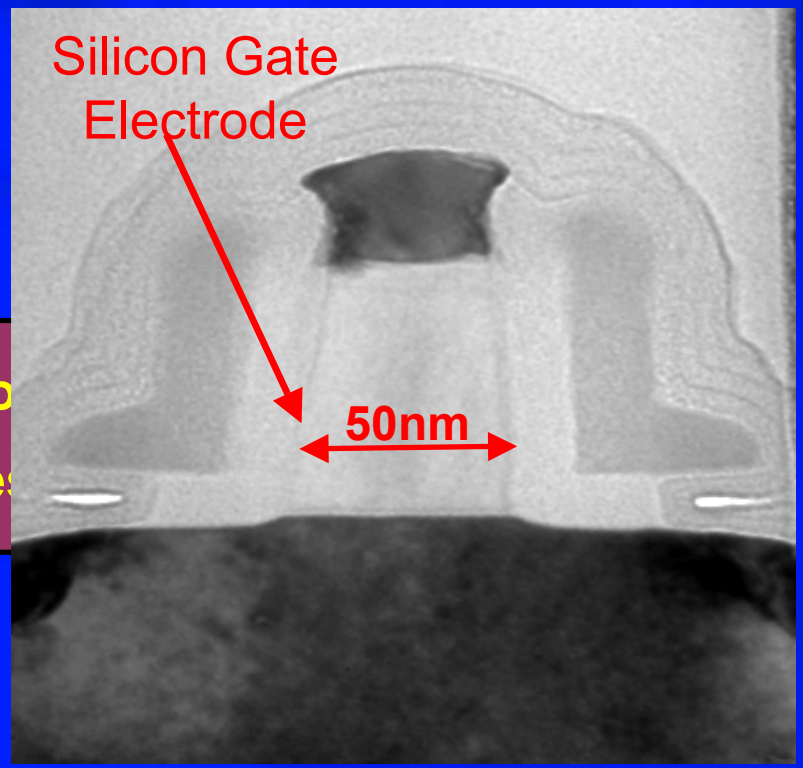
Gate feature size *uniformity* must be extremely tight across the whole mask. One bad gate can slow down or short out the entire chip.

World Leading Transistor Gate Patterning Capability

- Industry leading 50nm transistor: small gate patterning
- World best mask gate CD (critical dimension) uniformity
  - 12 nm vs. ~20 nm industry typical



Gate Mask for
50nm Transistor



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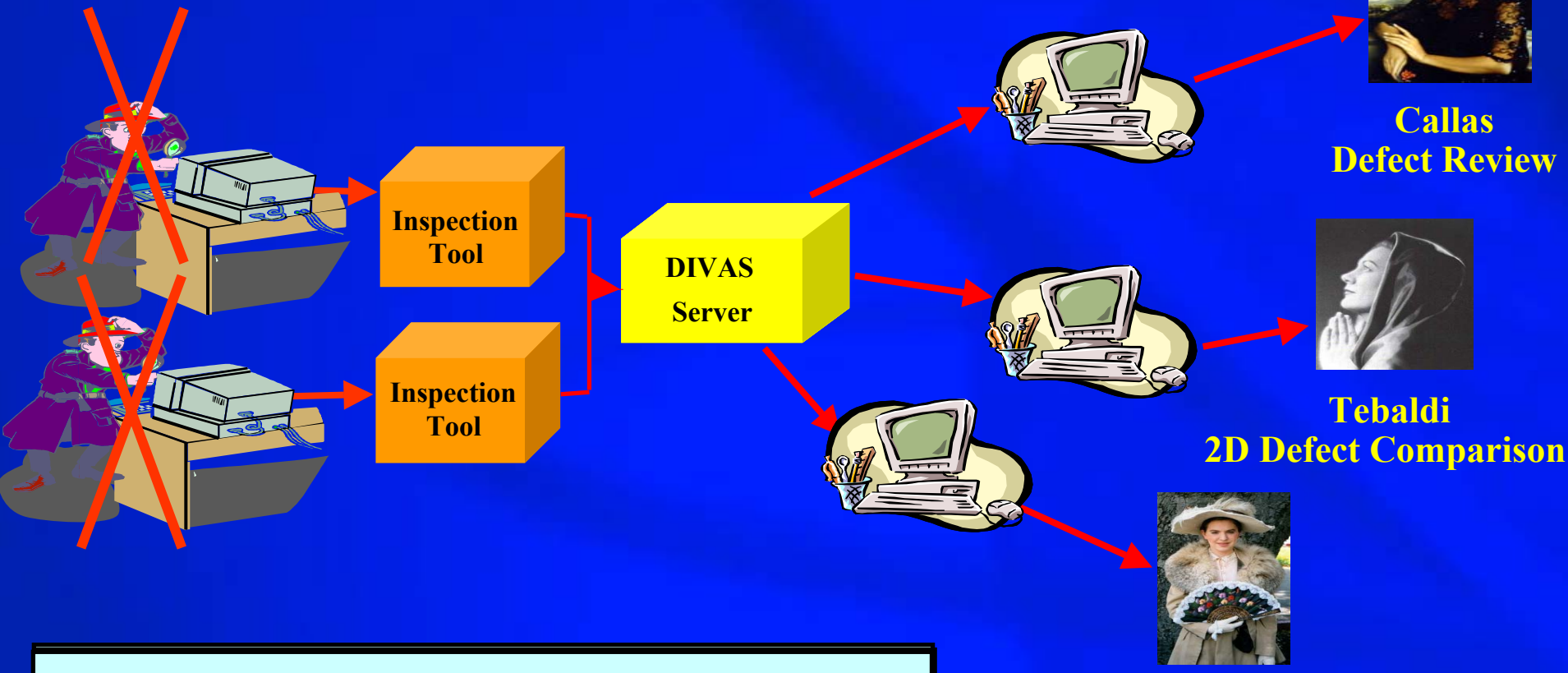
Industry Leading Mask Defect Management System

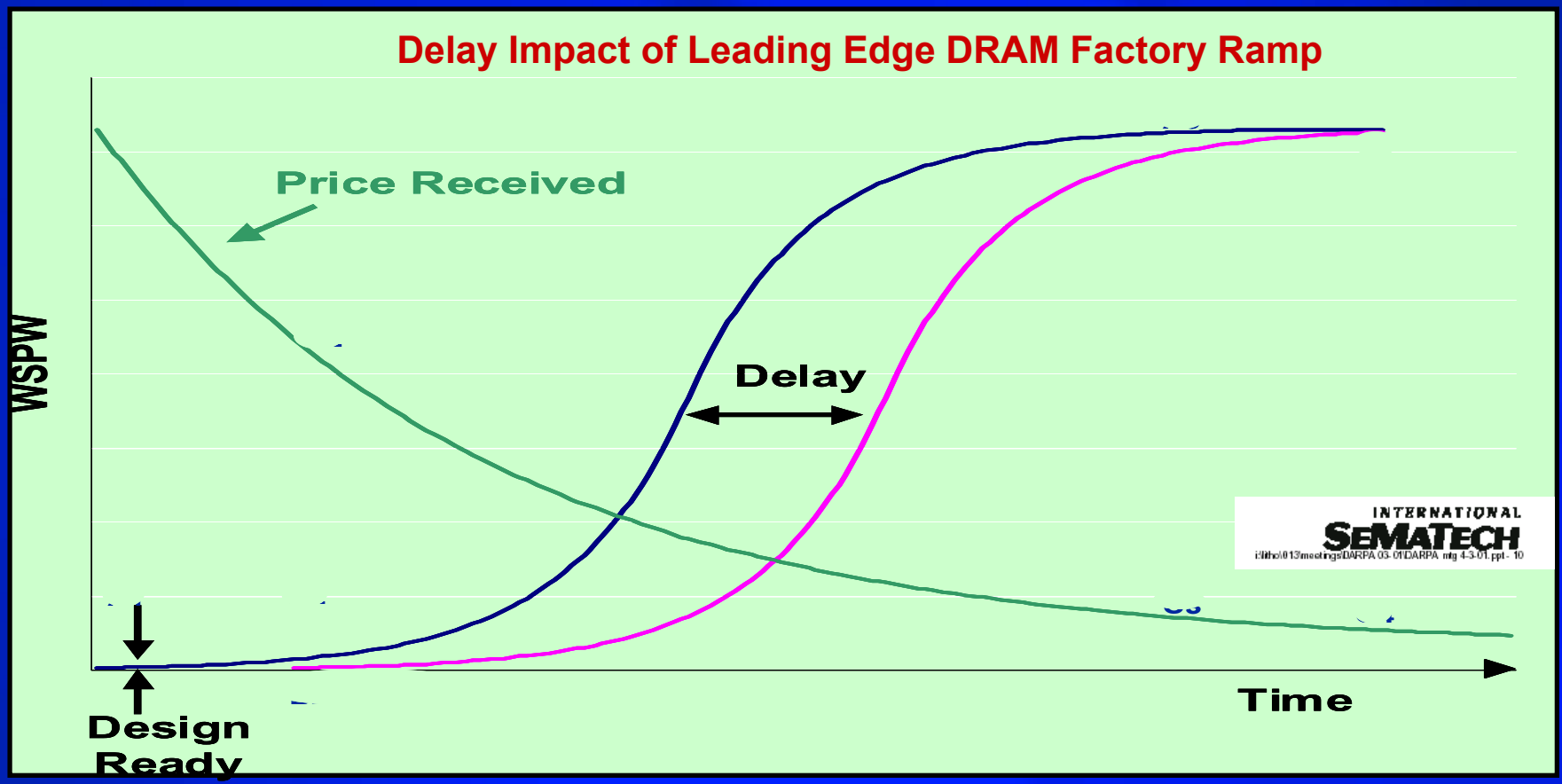
Defect management is critical for mask yield & quality



An Intel Unique Capability

Find all the "Basketballs"

IMO World Class Throughput Time: Time-to-Money Advantages

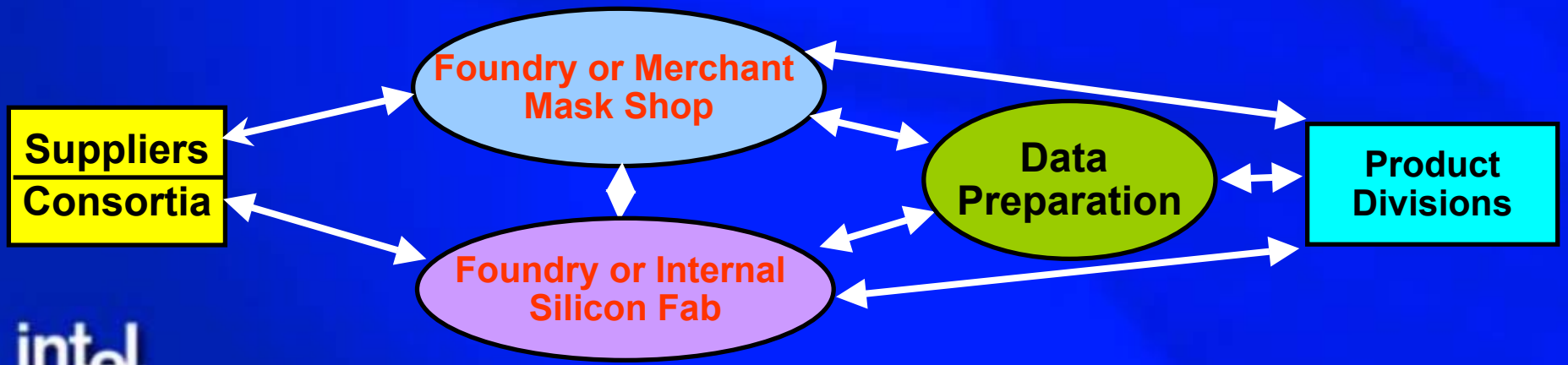


- ~ $2.5M/day delay impact for new product introduction
- IMO "priority" mask delivery TPT ***the best*** in the world
  - 5 days for the first 3 layers (130nm node)
  - Merchant mask shops 7-12 days

Integrated Mask Services & Solutions

- Intel streamlined supply chain & one-stop-shop services

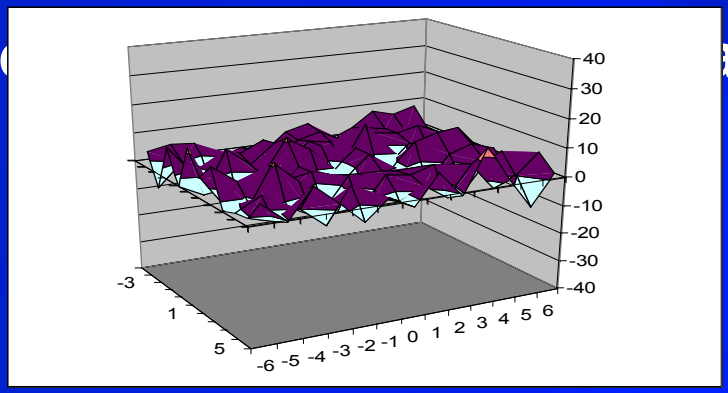
- Industry typical structure:



Integrated Mask Services & Solution

- **Organizational synergy and optimized solutions**
  - Mask shop, Design and Lithography work closely & unconstrained
  - Example: E-beam mask correction for wafer, an ***Intel Unique Capability***
- **Str… …and on…**

Feature Size Variation



"Perfect" mask

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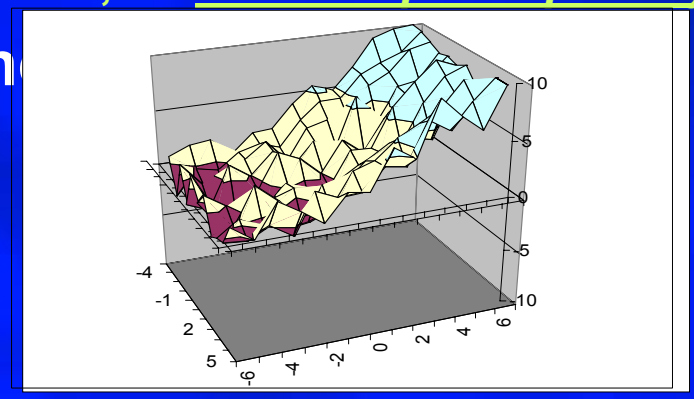

Systematic errors on wafer

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Rapid Feedback Loop
Design, Litho, Mask

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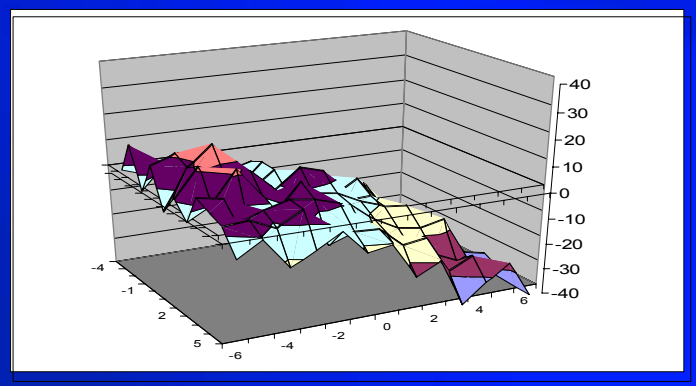

Reversed mask compensation

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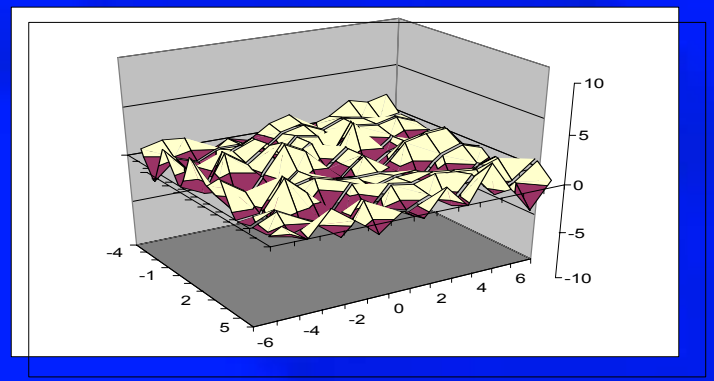
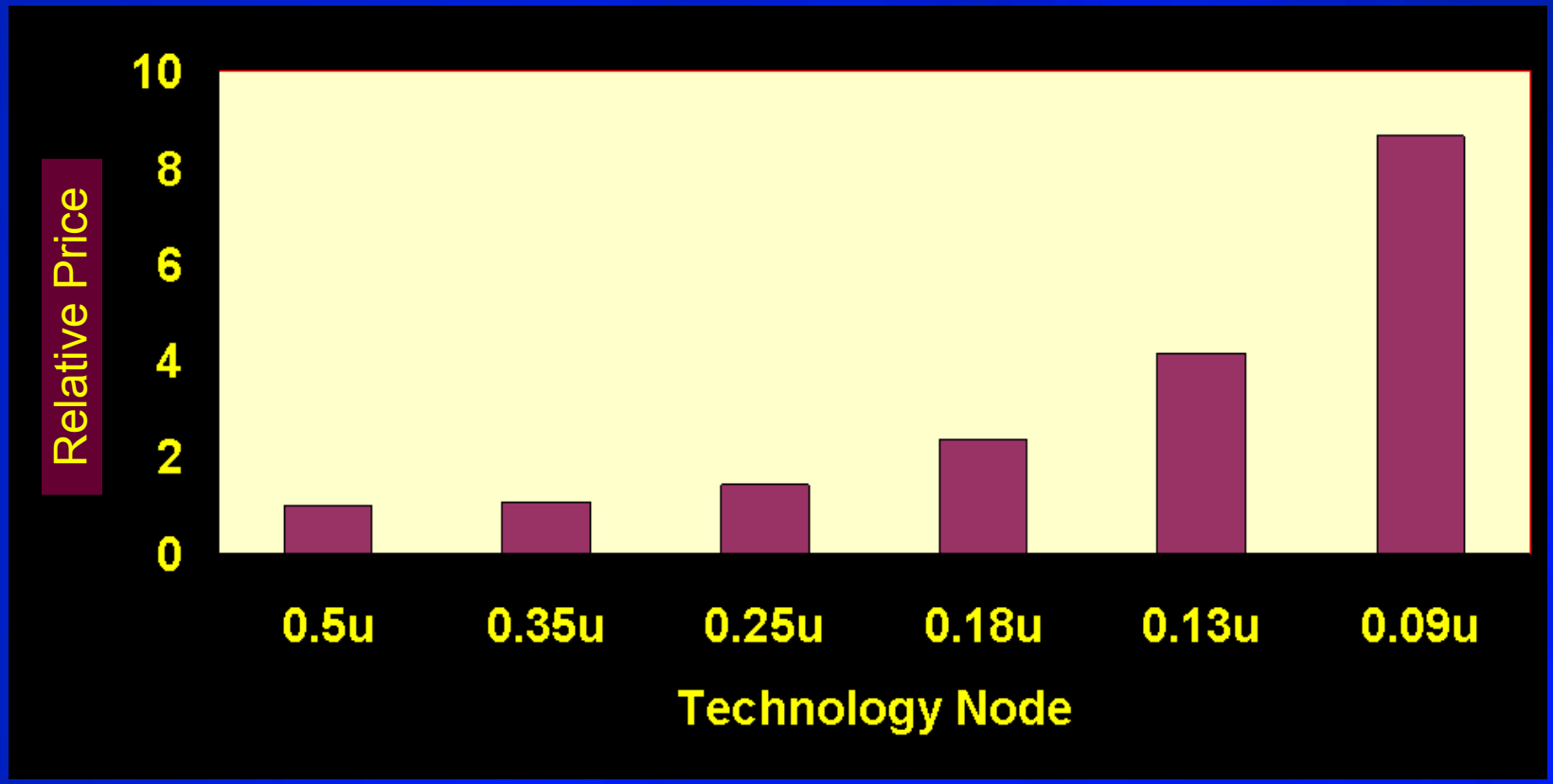


"Perfect" wafer

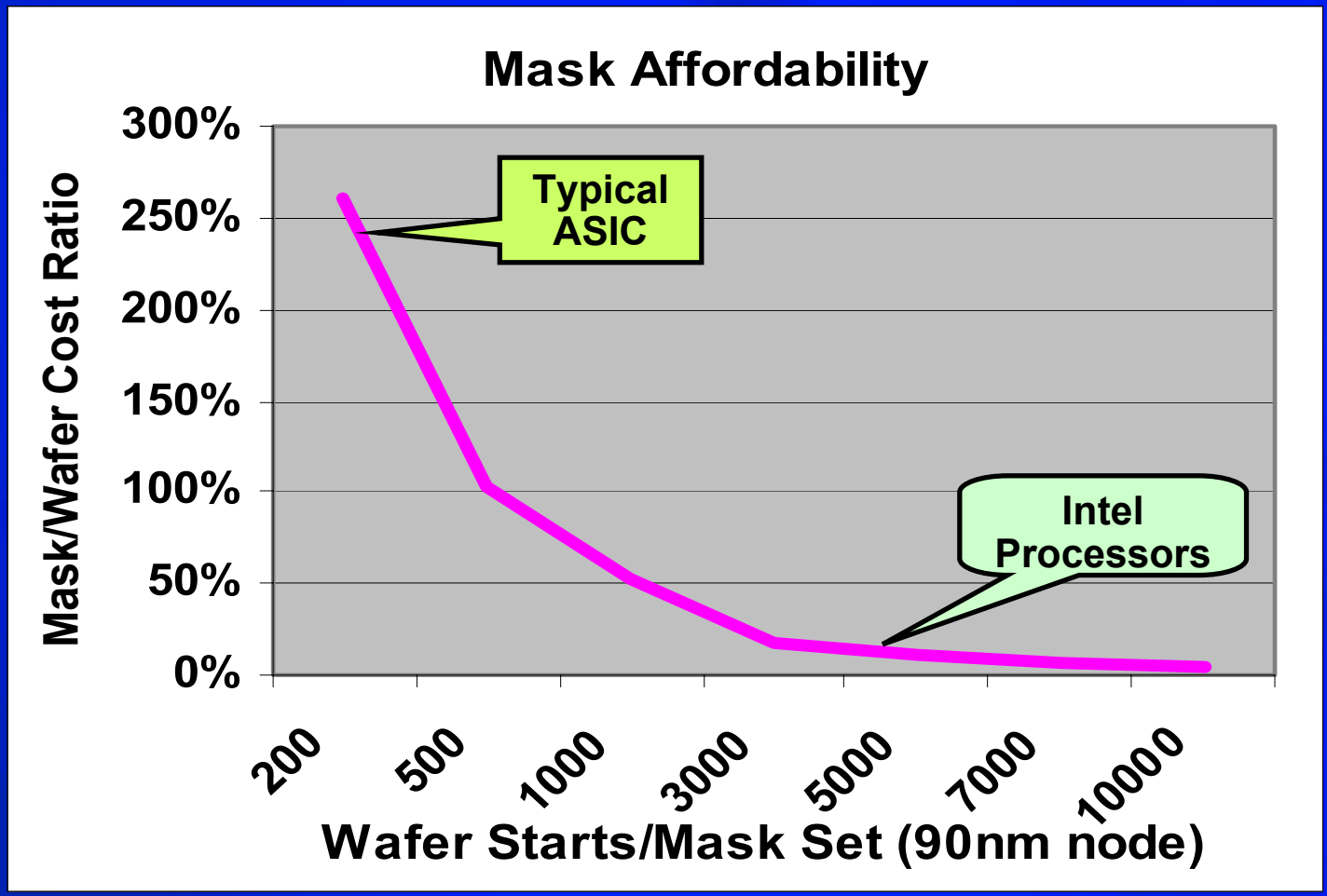
Trend of Mask Set Price



- Resolution Enhancement Techniques is a main driver for this trend
- IC foundry and mask merchant: ***$1.0-1.5M*** per 90nm mask set

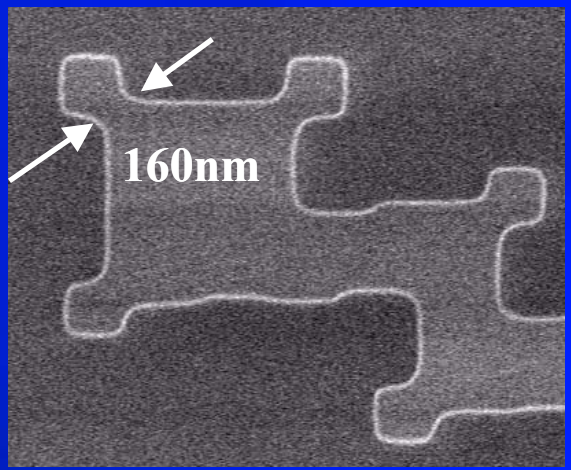
Three Cost Advantages for Intel Masks

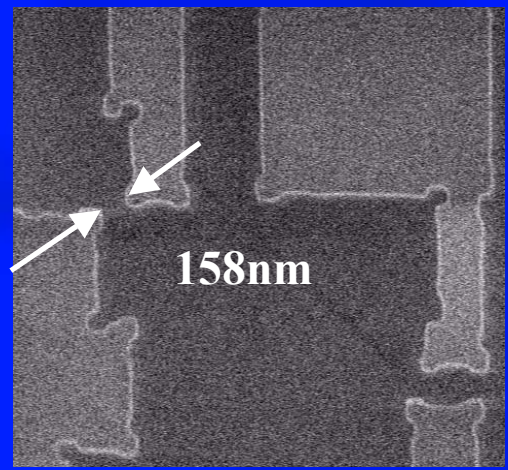
- Intel high-end mask cost < < merchant price (due to yield & cost margins)
- Intel mainstream products are high volume ⇒ excellent ***Affordability***
- Mask shuttle solution in place for low volume products



Intel 65nm Node Mask Leadership

- Intel is well into 65nm node Silicon development
- IMO delivered a *full set of critical masks* in Q4/02
  - Has been providing 65nm node test masks since Q1/02
  - Delivering a full set of *device quality* masks in Q1/03
- World leading capability and on track for 2 year cycle
  - Advanced 193nm wavelength Resolution Enhanced Masks (low K1)
  - *< 260nm main features* (< 65nm on wafer) and < 160nm sub-features
  - Excellent mask CD (critical dimension) *uniformity of <10.5nm*





65nm Node Masks with Sub-Features < 160nm (4X)

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